RL78/F13, F14

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DTC Usage Example (High-Speed Transfer and Chain Transfer)

Summary

This document describes the use of the DTC (high-speed transfer and chain transfer). It explains how to use the end of A/D conversion as the DTC trigger to transfer (high-speed transfer) the A/D conversion result to RAM, to perform a serial transmission (chain transfer) of the A/D conversion result to UART0, and to reflect (chain transfer) the A/D conversion result in the PWM output width.

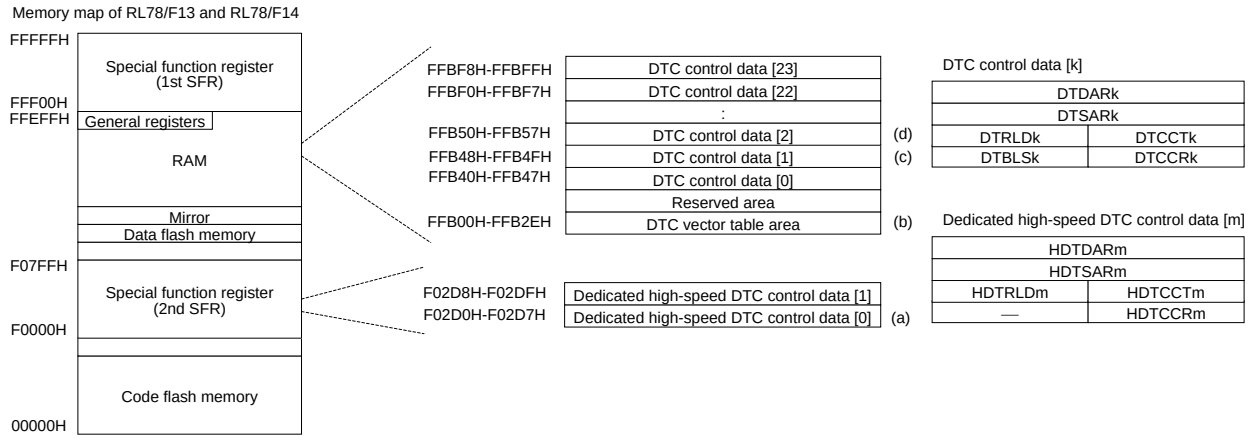
Contents

1. Overview of DTC (High-Speed Transfer and Chain Transfer) Operation

The DTC of the RL78/F13 and RL78/F14 provides functionality for transferring data between areas of memory without using the CPU. There are two transfer methods: normal transfer, in which the control data is located in RAM, and high-speed transfer, which uses dedicated control data registers to allow for fewer transfer cycles than normal transfer. There are also two transfer modes (normal mode and repeat mode), and a chain transfer function that automatically continues after a transfer finishes with the next specified transfer.

During the DTC (high-speed transfer and chain transfer) operation, the DTC (high-speed transfer) initially takes place when a DTC activation source is generated. When chain transfer is enabled, the next DTC (normal transfer) then takes place and chain transfers continue until a DTC transfer with chain transfer disabled completes. All chain transfers use the normal DTC transfer method. A DTC transfer-end interrupt request is output when the first DTC (high-speed transfer) is executed, but the interrupt is held pending during DTC chain transfers. Thus, the DTC transfer-end interrupt can be accepted only when all transfers have finished.

Figure 1.1 is an outline of DTC (high-speed transfer and chain transfer) operation, and Figure 1.2 to Figure 1.5 are flowcharts of DTC (high-speed transfer and chain transfer) internal operation.



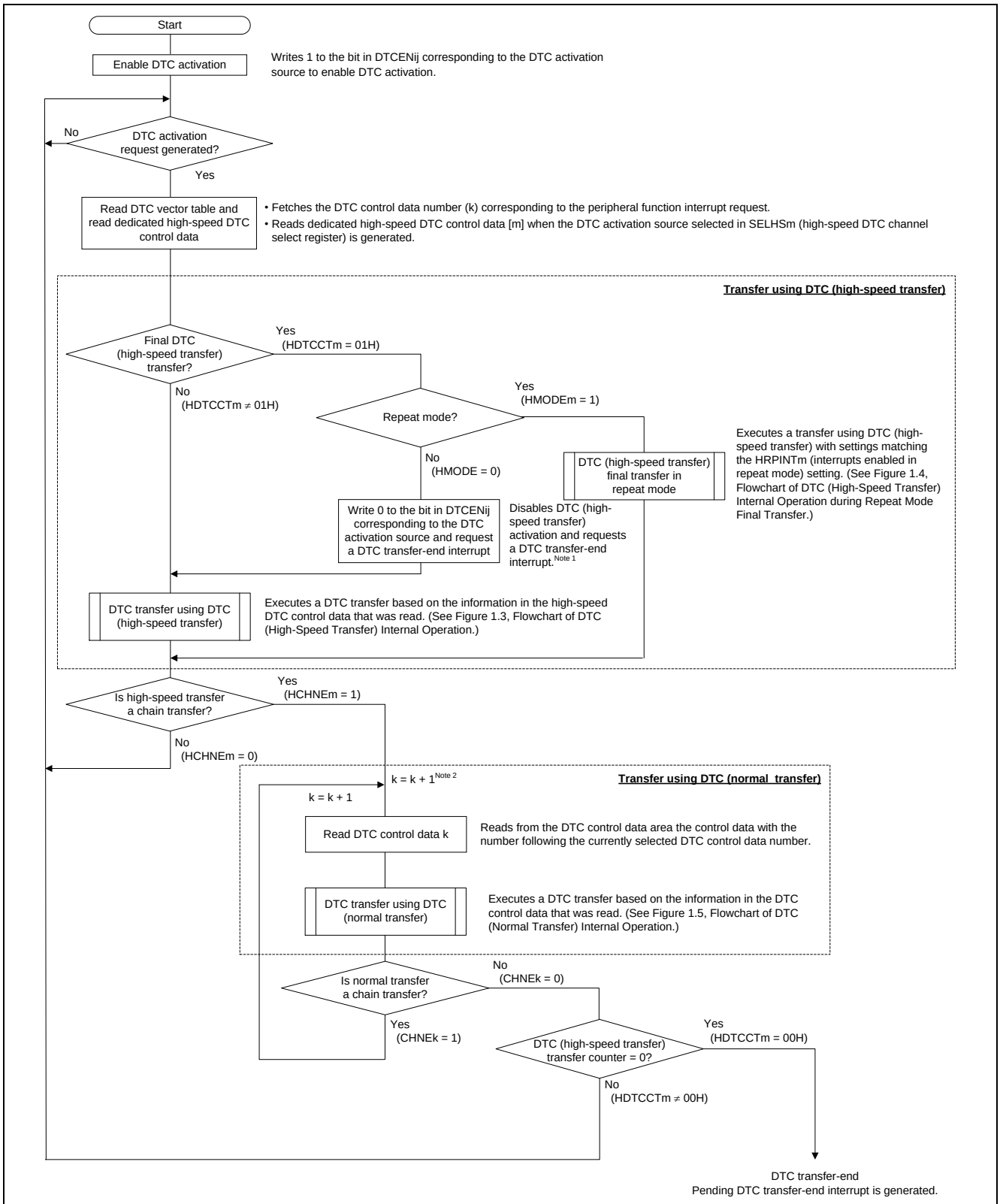
The operation described below occurs when the following settings are made: Chain transfer enabled on DTC (high-speed channel 0), “40H” stored in DTC vector table area corresponding to DTC activation source, chain transfer enabled in DTC control data [1], and chain transfer disabled in DTC control data [2].

1. Event selected as DTC activation source of DTC (high-speed channel 0) occurs.
2. Dedicated high-speed DTC control data [0] is read and a memory transfer takes place (a).
3. Control data [0] indicates that the value read from the DTC vector table area (b) corresponding to the activation source is “40H (k = 0).” When chain transfer starts, the next data, DTC control data [1], is read and a memory transfer takes place (c).
4. Next DTC control data [2] is read and a memory transfer takes place (d). Chain transfer is disabled in DTC control data [2], so chain transfer corresponding to the DTC activation source ends.

Note Values in the figure for the DTC vector table area and the addresses indicated by DTC control data apply when the setting of the DTCBAR register is “FBH.”

Remarks k = 0 to 23, m = 0 or 1

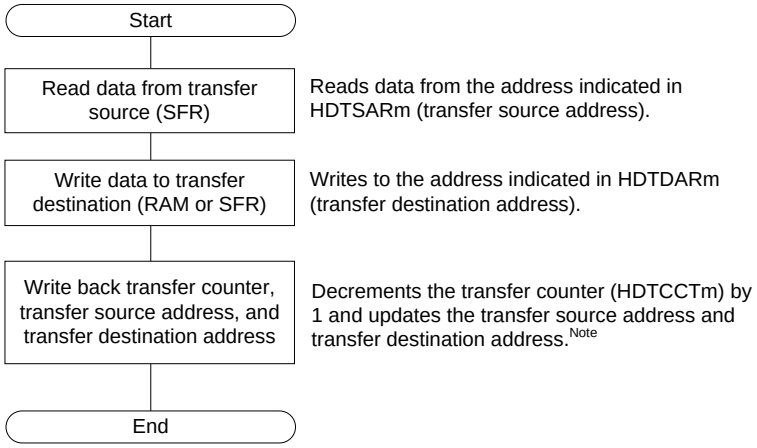
Figure 1.1 Flowchart (Outline) of DTC (High-Speed Transfer and Chain Transfer) Operation



Notes 1. Interrupts are held pending until all chain transfers complete.
2. The DTC control data read first during chain transfer operation is the control data with the number equal to the DTC control data number (k) selected when the DTC activation request was generated + 1.
3. The peripheral function interrupt selected as the DTC (high-speed transfer) activation source is generated.

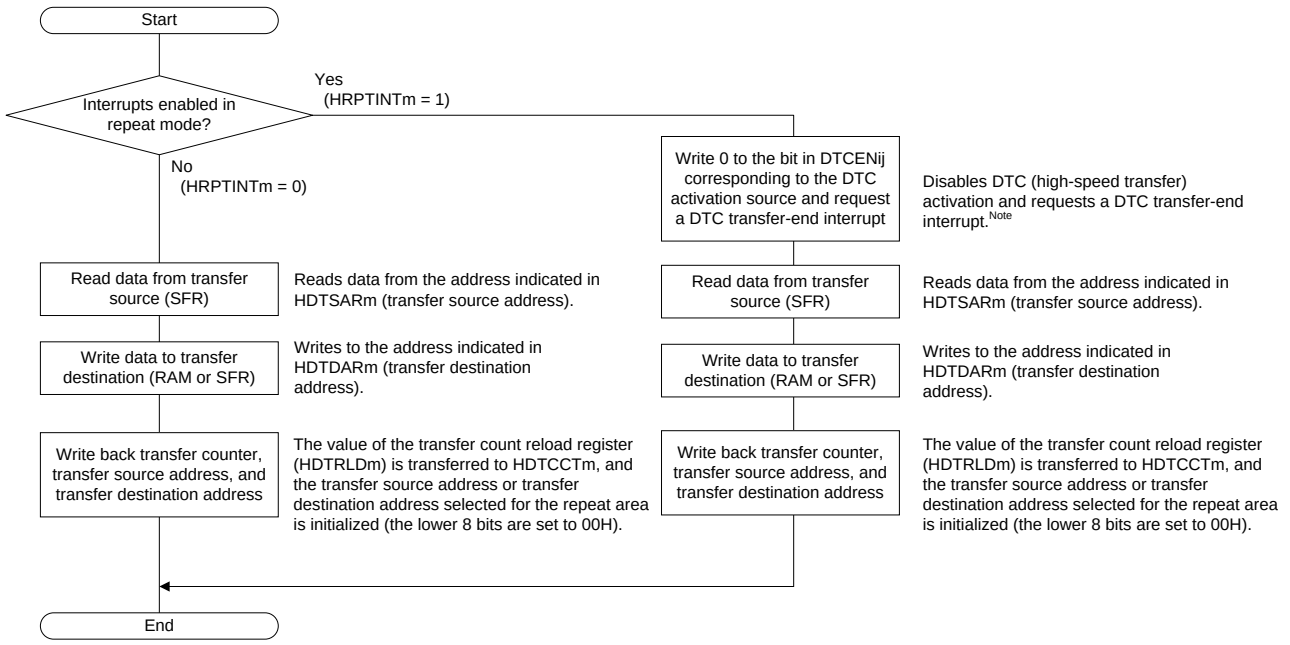
Remarks i = 0 to 5, j = 0 to 7, k = 0 to 23, m = 0 or 1

Figure 1.2 Flowchart of DTC (High-Speed Transfer and Chain Transfer) Internal Operation



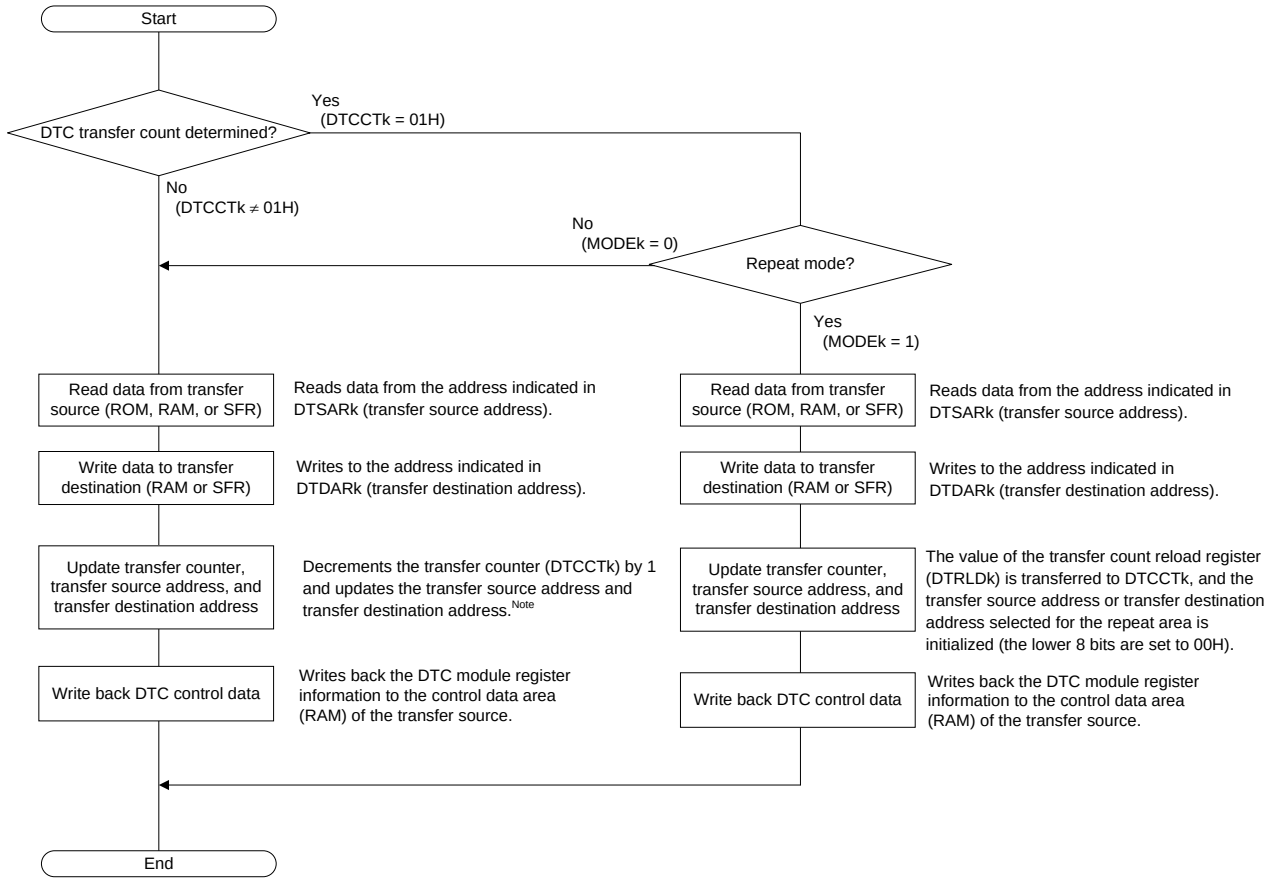
Notes Address control is set to “incremented,” and 1 is added for 8-bit transfers.
Address control is set to “incremented,” and 2 is added for 16-bit transfers.
Remarks m = 0 and 1

Figure 1.3 Flowchart of DTC (High-Speed Transfer) Internal Operation



Note Interrupts are held pending until all chain transfers complete.
Remarks i = 0 to 5, j = 0 to 7, m = 0 or 1

Figure 1.4 Flowchart of DTC (High-Speed Transfer) Internal Operation during Repeat Mode Final Transfer



Notes Address control is set to “incremented,” and 1 is added for 8-bit transfers.
Address control is set to “incremented,” and 2 is added for 16-bit transfers.

Remarks k = 0 to 23
When using chain transfer with DTC (high-speed transfer), the setting of the RPTINTk bit (interrupt setting for repeat mode) of the control data area has no effect.

Figure 1.5 Flowchart of DTC (Normal Transfer) Internal Operation

2. Specifications

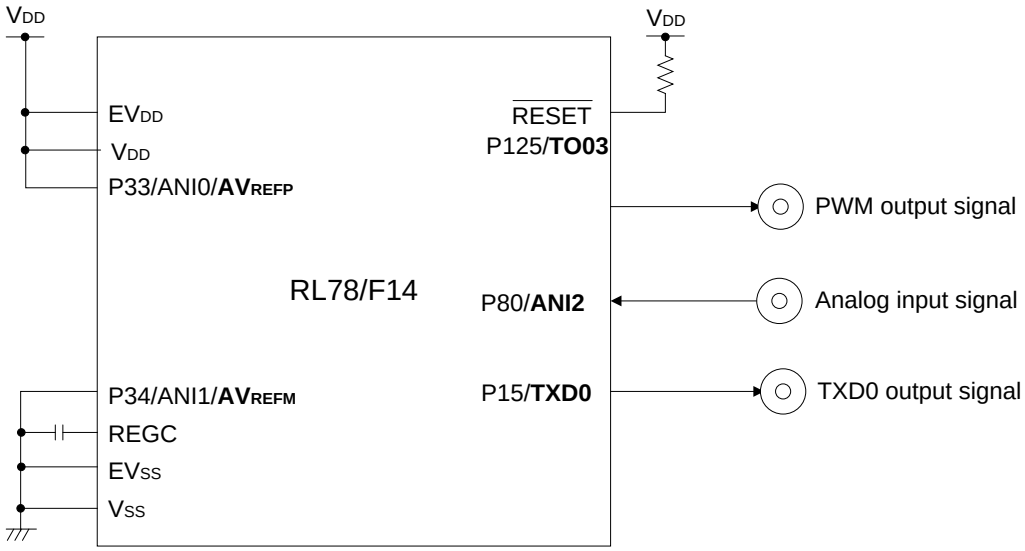
A usage example combining the DTC, the A/D converter, timer array unit (TAU) channels 0 to 3 (TAU00 to TAU03), and UART0 transmission (on channel 0 (SAU00) of the serial array unit (SAU)) is presented below.

TAU00 (2.04 ms) and TAU01 (1.02 ms) count in coordinated fashion, and the A/D converter uses the TAU01 interrupt request signal as the trigger to perform A/D conversion of the input voltage on the ANI2 pin. In addition, TAU02 (510 μs) and TAU03 count in coordinated fashion, and a PWM signal is output on the TO03 pin. Using the A/D conversion end as the DTC (high-speed transfer) activation source, the DTC starts operating and performs the following memory transfers by means of chain transfers:

- Transfer of the A/D conversion result to RAM (DTC (high-speed transfer))
- Transfer of the A/D conversion result stored in RAM to the SDR00L register (DTC (normal transfer))
- Transfer of the A/D conversion result stored in RAM to the TDR03 register (DTC (normal transfer))

After this, the above processing is repeated.

Figure 2.1 is a connection diagram showing the pins used, Table 2.1 lists the peripheral functions used and their applications, Figure 2.2 is a configuration diagram of the peripheral functions used, Figure 2.3 shows the allocation of the DTC control data and DTC vector table, and Figure 2.4 and Figure 2.5 show the DTC transfer timing.



In the application described in this document AV_{REFP}, AV_{REFM}, ANI2, TO03, and TXD0 are used.

Figure 2.1 Connection Diagram of Pins Used

Table 2.1 Peripheral Functions Used and Their Applications

Peripheral Function	Application
A/D converter	Performs A/D conversion on the analog input signals from channel ANI2. 8-bit resolution Hardware trigger no-wait mode (source: INTTM01) Select mode (1-channel) One-shot conversion mode
TAU00	Constant-period timer Interval timer mode (2.04 ms) Used as master channel
TAU01	Generates A/D conversion trigger (INTTM01). One-count mode (1.02 ms) Used as TAU00 slave channel.
TAU02	Constant-period timer Interval timer mode (510 μs) Used as master channel
TAU03	PWM signal output One-count mode Output pin: TO03 High width: 0 to 510 μs (zero-expanded data derived from upper 8 bits of A/D conversion result) Used as TAU02 slave channel
SAU00	Performs transmission on TXD0 pin in UART mode. Operating mode: UART mode (transmit function) Baud rate: 9,600 bps (error: +0.16%) (8 data bits, no parity, 1 stop bit, LSB-first)
DTC (high-speed DTC channel 0)	Transfers the A/D conversion result register value to the RAM. DTC activation source: End of A/D conversion Transfer source address: ADCRH register Transfer destination address: RAM Transfer size: 1 byte Transfer count: 1 Operating mode: Repeat mode, chain transfer enabled
DTC (control data 1)	Transfers the A/D conversion result register value to serial data register 00. DTC activation source: — Transfer source address: RAM (A/D conversion result storage destination) Transfer destination address: SDR00L register Transfer size: 1 byte Transfer count: 1 Operating mode: Repeat mode, chain transfer enabled
DTC (control data 2)	Transfers the A/D conversion result register value to timer data register 03. DTC activation source: — Transfer source address: RAM (A/D conversion result storage destination) Transfer destination address: TDR03 register Transfer size: 2 bytes Transfer count: 1 Operating mode: Repeat mode, chain transfer disabled

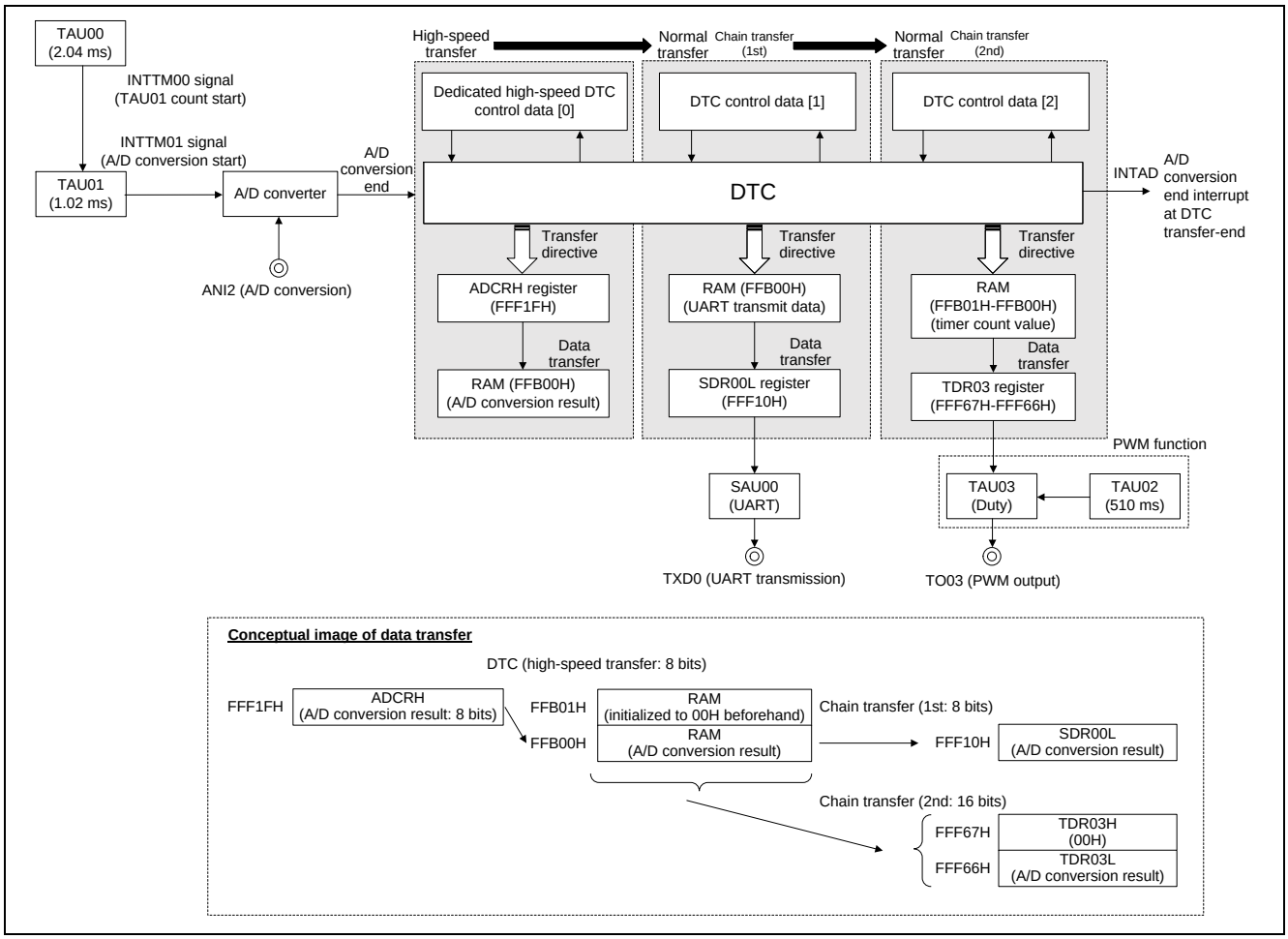


Figure 2.2 Configuration Diagram of Peripheral Functions Used

(SFR area)

F02DEH	HDTDAR1		Dedicated high-speed DTC control data [1]
F02DCH	HDTSAR1		
F02DAH	HDTRLD1	HDTCCT1	
F02D8H	—	HDTCCR1	
F02D6H	HDTDAR0		Dedicated high-speed DTC control data [0]
F02D4H	HDTSAR0		
F02D2H	HDTRLD0	HDTCCT0	
F02D0H	—	HDTCCR0	

(RAM area)Note 1

+F8 to +FFH	Control data [23]		
+F0 to +F7H	Control data [22]		
:	:		
+58 to +5FH	Control data [3]		
+56H	DTDAR2		Control data [2]
+54H	DTSAR2		
+52H	DTRLD2	DTCCT2	
+50H	DTBLS2	DTCCR2	
+4EH	DTDAR1		Control data [1]
+4CH	DTSAR1		
+4AH	DTRLD1	DTCCT1	
+48H	DTBLS1	DTCCR1	
+46H	DTDAR0		Control data [0]
+44H	DTSAR0		
+42H	DTRLD0	DTCCT0	
+40H	DTBLS0	DTCCR0	
+2EH to +3FH	Reserved area		
+2CH	(INTTM17)	(INTTM16)	DTC vector table area
+2AH	(INTTM15)	(INTTM14)	
+28H	(INTLIN1TRM)	(INTLIN1RVC)	
+26H	(INTTM13)	(INTTM12)	
+24H	(INTTM11)	(INTTM10)	
+22H	(INTCMP0)	(INTRJ0)	
+20H	(TRDSR1.IMFD)	(TRDSR1.IMFC)	
+1EH	(TRDSR1.IMFB)	(TRDSR1.IMFA)	
+1CH	(TRDSR0.IMFD)	(TRDSR0.IMFC)	
+1AH	(TRDSR0.IMFB)	(TRDSR0.IMFA)	
+18H	(INTTM07)	(INTTM06)	
+16H	(INTTM05)	(INTTM04)	
+14H	(INTTM03)	(INTTM02)	
+12H	(INTTM01)	(INTTM00)	
+10H	—	(INTCANGRFR)	
+0EH	(INTLIN0TRM)	(INTLIN0RVC)	
+0CH	(INTST1)Note 2	(INTSR1)Note 3	
+0AH	(INTST0)Note 4	(INTSR0)Note 5	
+08H	(INTAD)	(INTKR)	
+06H	(INTP6)	(INTP5)	
+04H	(INTP4)	(INTP3)	
+02H	(INTP2)	(INTP1)	
+00H	(INTP0)	—	

Notes 1. The DTC (normal transfer) control data and DTC vector table are allocated in RAM. The start address is set in the DTCBAR register.
2. INTST1/INTCSI10/INTIIC10
3. INTSR1/INTCSI11/INTIIC11
4. INTST0/INTCSI00/INTIIC00
5. INTSR0/INTCSI01/INTIIC01

Figure 2.3 Allocation of DTC Control Data and DTC Vector Table

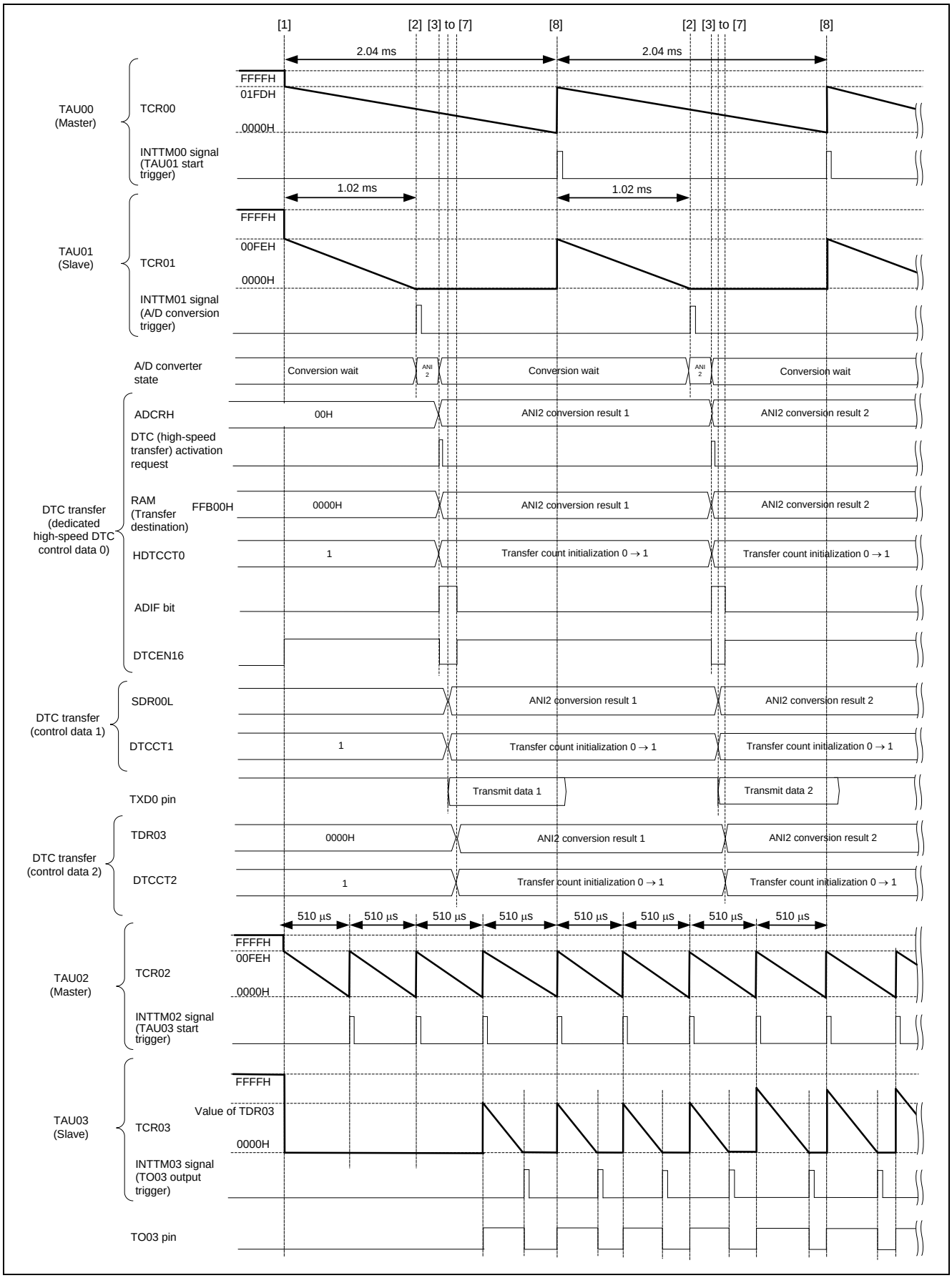


Figure 2.4 DTC Transfer Timing (1/2)

[1] The following register settings are made by the software to put the function in the operational state:
- The DTCEN16 bit in the DTCEN1 register is set to 1 (DTC activation enabled (source: A/D conversion end)).
- The TS00, TS01, TS02, and TS03 bits in the TS0 register are set to 1 (start counting on TAU00, TAU01, TAU02, and TAU03).
- The SE00 bit in the SS0 register is set to 1 (SAU0 CH0 in transmit-standby state).

[2] When TAU01 finishes counting, the INTTM01 signal is output. Also, A/D conversion starts, using this signal as the trigger.

[3] After A/D conversion end, the ADIF bit changes to 1 and a DTC (high-speed transfer) memory transfer is performed (ADCRH register → RAM), using the A/D conversion-end interrupt request signal as the trigger.
Also, the HDTCCT0 register is decremented when the DTC transfer occurs.

[4] When the transfer that causes the value of the HDTCCT0 register to change from 1 to 0 is executed, the following operations are performed:
- The DTCEN16 bit is cleared to 0 (DTC activation disabled).
- An A/D conversion-end interrupt request is generated due to the DTC (high-speed transfer) transfer end. (Generation of interrupts is held pending until all DTC transfers using chain transfer complete.)
- A data transfer using DTC (high-speed transfer) is executed (ADCRH register → RAM).
- The value of the HDTRLD0 register is stored in the HDTCCT0 register (initialization of transfer count using DTC (high-speed transfer)).

[5] After confirmation that the HCHNE0 bit in the HDTCCR0 register has been set to 1, control data 1 is read from the control data area and the following operations are performed:
- A data transfer using DTC (normal transfer) is executed (RAM (A/D conversion result storage area) → SDR00L register).
- The DTCCT1 register is decremented.

Also, SAU0 transmits the A/D conversion result on the TXD0 pin due to the data transfer to the SDR00L register.

[6] After confirmation that the CHNE bit in the DTCCR1 register has been set to 1, control data 2 is read from the control data area and the following operations are performed:
- A data transfer using DTC (normal transfer) is executed (RAM (16-bit extended value from A/D conversion result storage area) → TDR03 register).
- The DTCCT2 register is decremented.

[7] An A/D conversion-end interrupt request is generated due to the DTC transfer end. At this point the following settings are made by the software:
- The software sets the DTCEN16 bit in the DTCEN1 register to 1 (DTC (high-speed transfer) activation enabled).

[8] TAU00 and TAU01 perform the following operations:
- An INTTM00 signal is output when the TAU00 count completes (generation of TAU00 interrupt request signal).
- TAU01 (slave) starts counting.

Also, TAU02 and TAU03 perform the following operations during steps [2] to [8]:
- An INTTM02 signal is output when the TAU02 count completes (generation of TAU02 interrupt request signal), and the TO03 pin is driven to the high level (unless the value of the TDR03 register is 0000H).
- TAU03 (slave) starts counting.
- The TO03 pin is driven to the low level when the TAU03 count completes.

Notes TCR00: Timer counter register 00
INTTM00 signal: Timer channel 0 count-end/capture-end interrupt request signal
TCR01: Timer counter register 01
INTTM01 signal: Timer channel 1 count-end/capture-end interrupt request signal (Used as A/D conversion trigger.)
A/D conversion status: 10-bit successive approximation register
ADCRH: 8-bit A/D conversion result register (upper 8 bits of ADCR)
DTC (high-speed transfer) activation request: Single-channel A/D conversion-end interrupt signal
FFB00H: RAM indicating HDTDAR0 (high-speed DTC transfer destination address register) for A/D conversion result storage
HDTCCT0: High-speed DTC transfer count register 0
ADIF bit: A/D conversion end interrupt flag
DTCEN16: DTCEN16 bit in DTCEN1 register

SDR00L: Serial data register 00 (lower 8 bits of SDR00)
TXD0 pin: UART0 transmit pin
DTCCT1: DTC transfer count register 1 allocated in DTC control data area
TCR02: Timer counter register 02
INTTM02 signal: Timer channel 2 count-end/capture-end interrupt request signal
TCR03: Timer counter register 03
INTTM03 signal: Timer channel 3 count-end/capture-end interrupt request signal
TDR03: Timer data register 3
TO03 pin: Timer channel 3 PWM signal output pin
DTCCT2: DTC transfer count register 2 allocated in DTC control data area
CK03 (f_{CLK} / 128 = 250 kHz) selected as TAU00 and TAU01 count clock
CK02 (f_{CLK} / 64 = 500 kHz) selected as TAU02 and TAU03 count clock

Figure 2.5 DTC Transfer Timing (2/2)

3. Setting Procedures of Peripheral Functions

The setting procedures of the peripheral functions (DTC, A/D converter, TAU, and SAU), are described in this section.

3.1 Peripheral Function Initialization Procedure

Figure 3.1 shows the peripheral function initialization procedure.

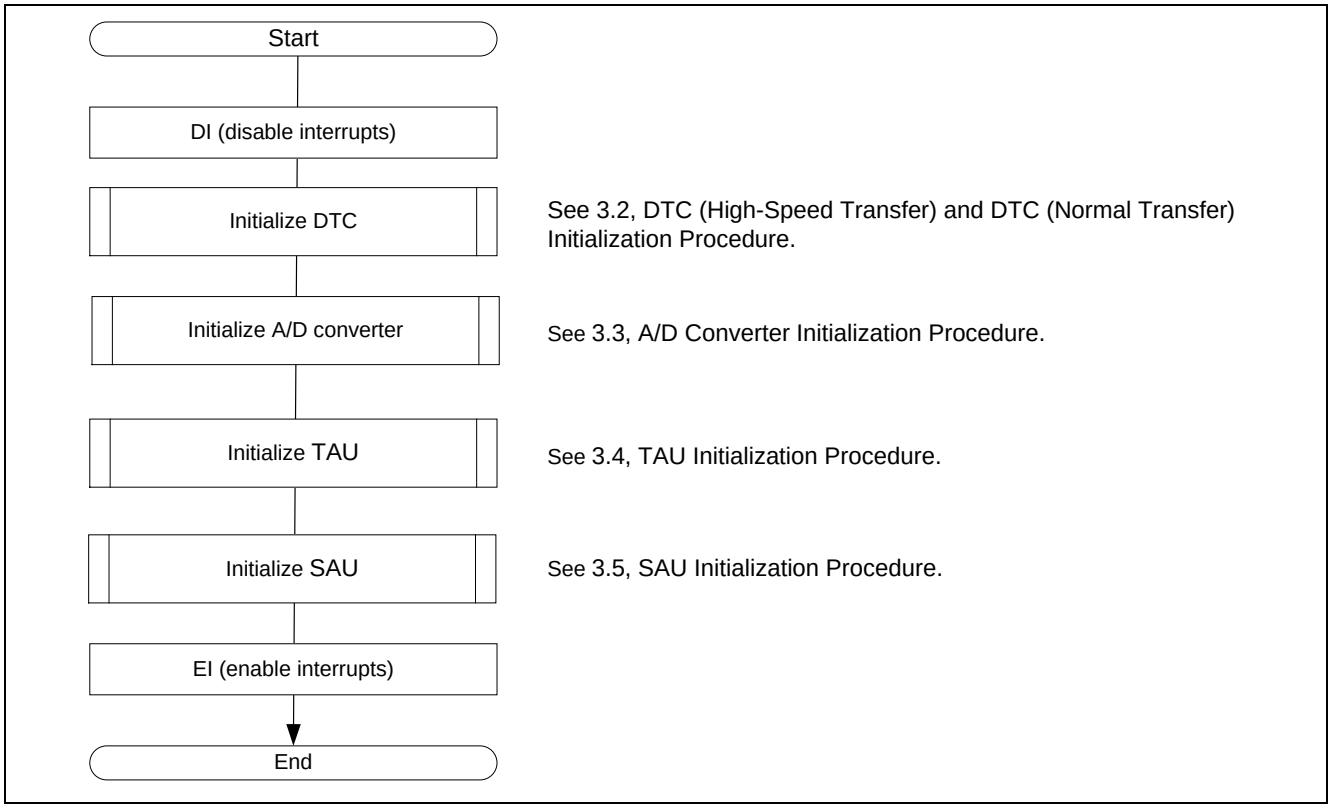


Figure 3.1 Peripheral Function Initialization Procedure

3.2 DTC (High-Speed Transfer) and DTC (Normal Transfer) Initialization Procedure

Using the end of A/D conversion as the activation source, the A/D conversion result is transferred (high-speed transfer) to the conversion result storage area in RAM, the A/D conversion result stored in the A/D conversion result storage area is transferred (chain transfer) to the SDR00L register, and the A/D conversion result stored in the A/D conversion result storage area (16-bit expanded) is transferred (chain transfer) to the TDR03 register, sequentially.

Figure 3.2 and Figure 3.3 show the DTC (high-speed transfer) and DTC (normal transfer) initialization procedure. Figure 3.4 shows the allocation of DTC control data.

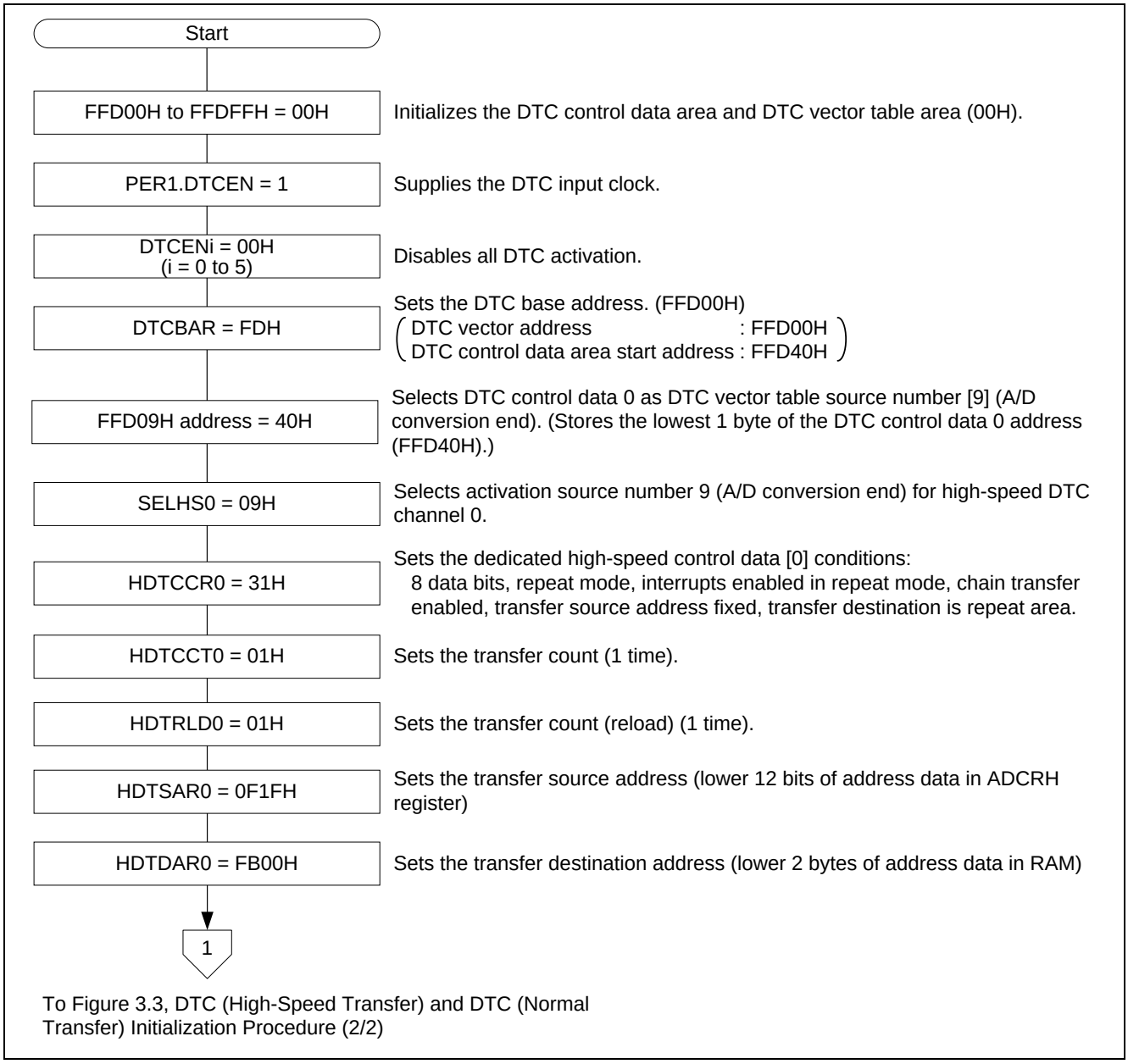


Figure 3.2 DTC (High-Speed Transfer) and DTC (Normal Transfer) Initialization Procedure (1/2)

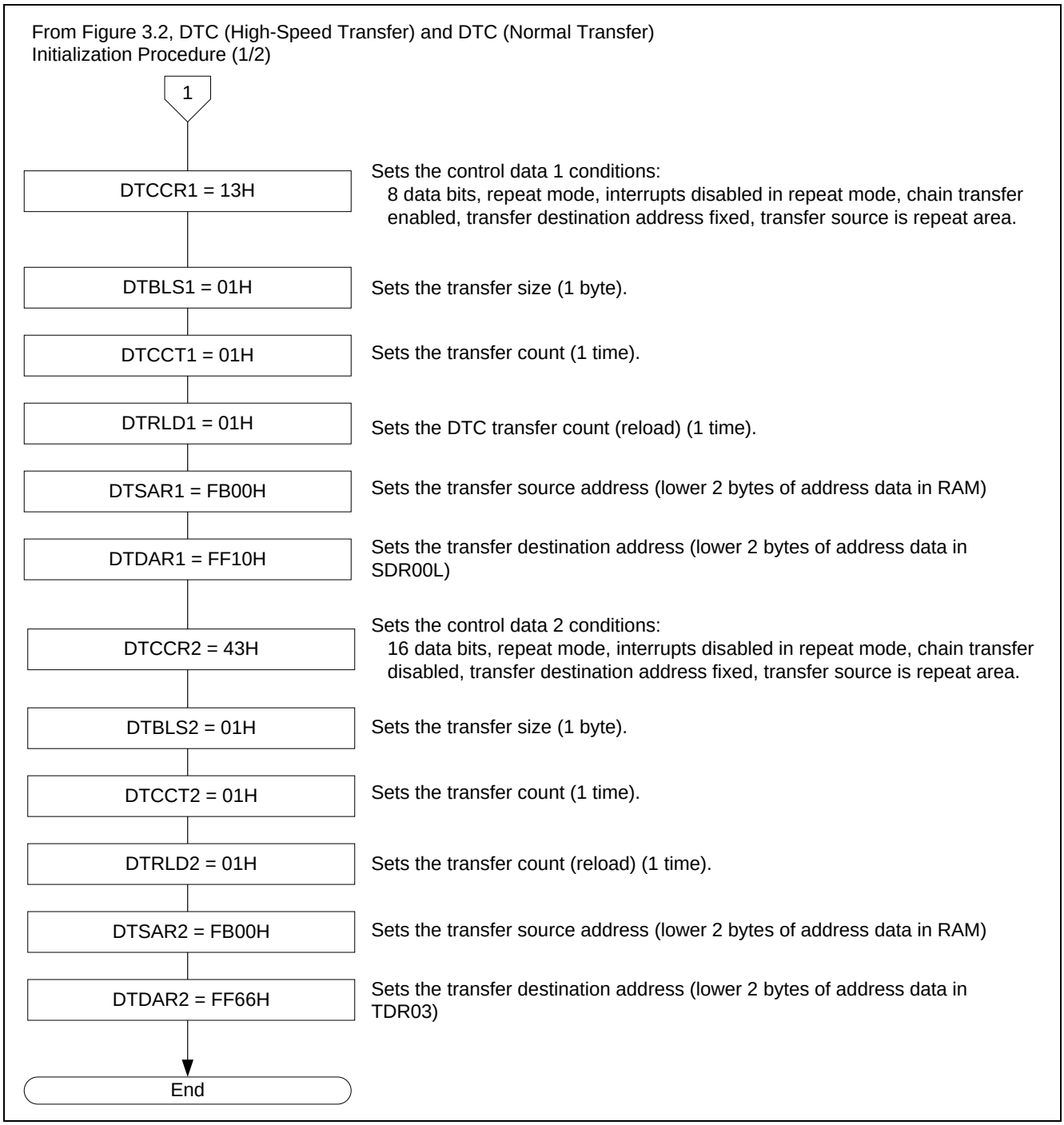
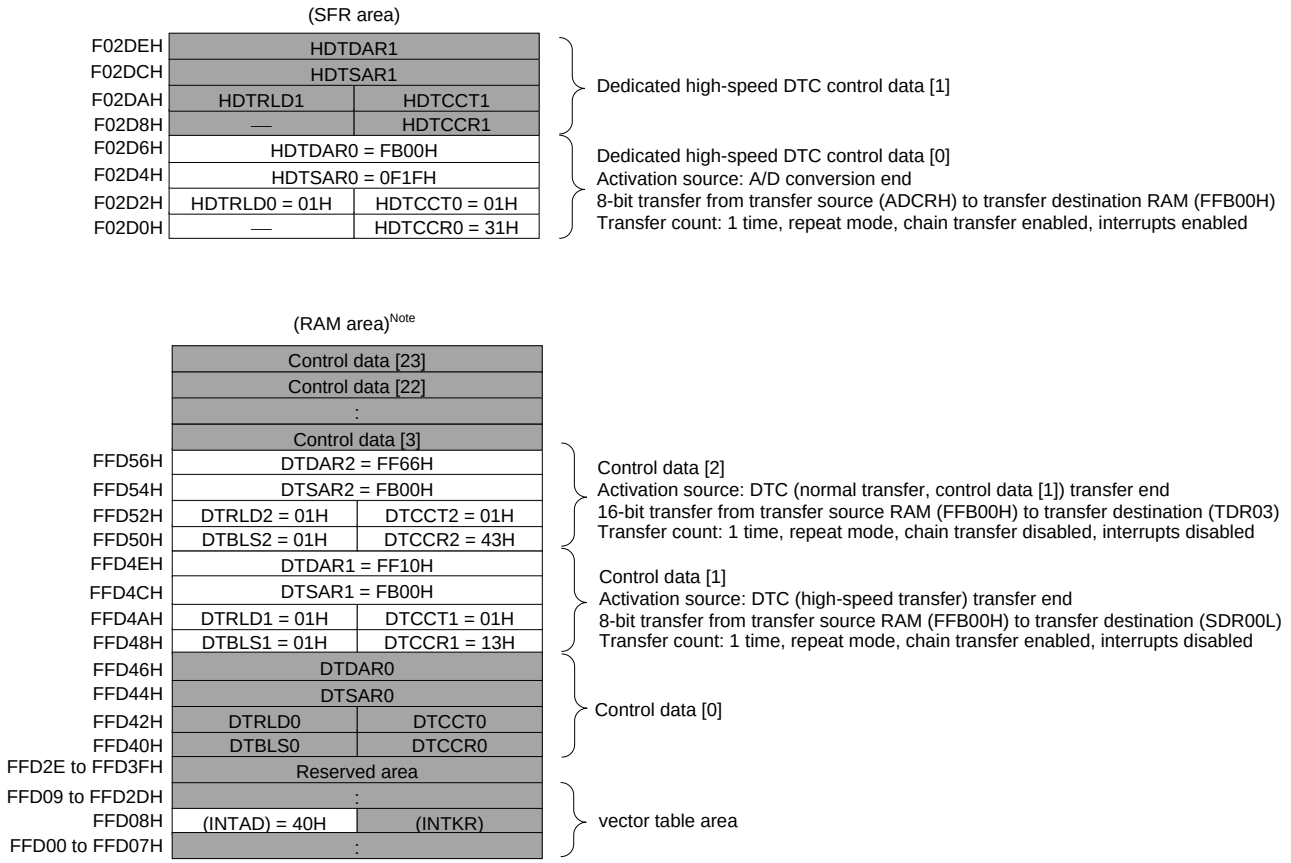


Figure 3.3 DTC (High-Speed Transfer) and DTC (Normal Transfer) Initialization Procedure (2/2)



Note When FDH is set in the DTCBAR register (DTC control data and DTC vector table start address set to FFD00H).

Remarks In the example presented in this document, the DTC activation source (INTAD) causes the register information stored in dedicated high-speed DTC control data [0] to be read and DTC (high-speed transfer) to take place based on that register information.
The register information read from dedicated high-speed DTC control data [0] indicates that chain transfer is enabled, so the register information stored in the next control data (in this case, control data [1]) is read, and based on that register information DTC (normal transfer) takes place.
The register information read from control data [1] also indicates that chain transfer is enabled, so the register information stored in the next control data (in this case, control data [2]) is read, and based on that register information DTC (normal transfer) takes place.
The register information read from control data [2] indicates that chain transfer is disabled, so DTC chain transfer ends.

Figure 3.4 Allocation of DTC Control Data

3.3 A/D Converter Initialization Procedure

The following settings are used to perform A/D conversion of the analog input signals on channel ANI2.

Figure 3.5 shows the initialization procedure for the A/D converter.

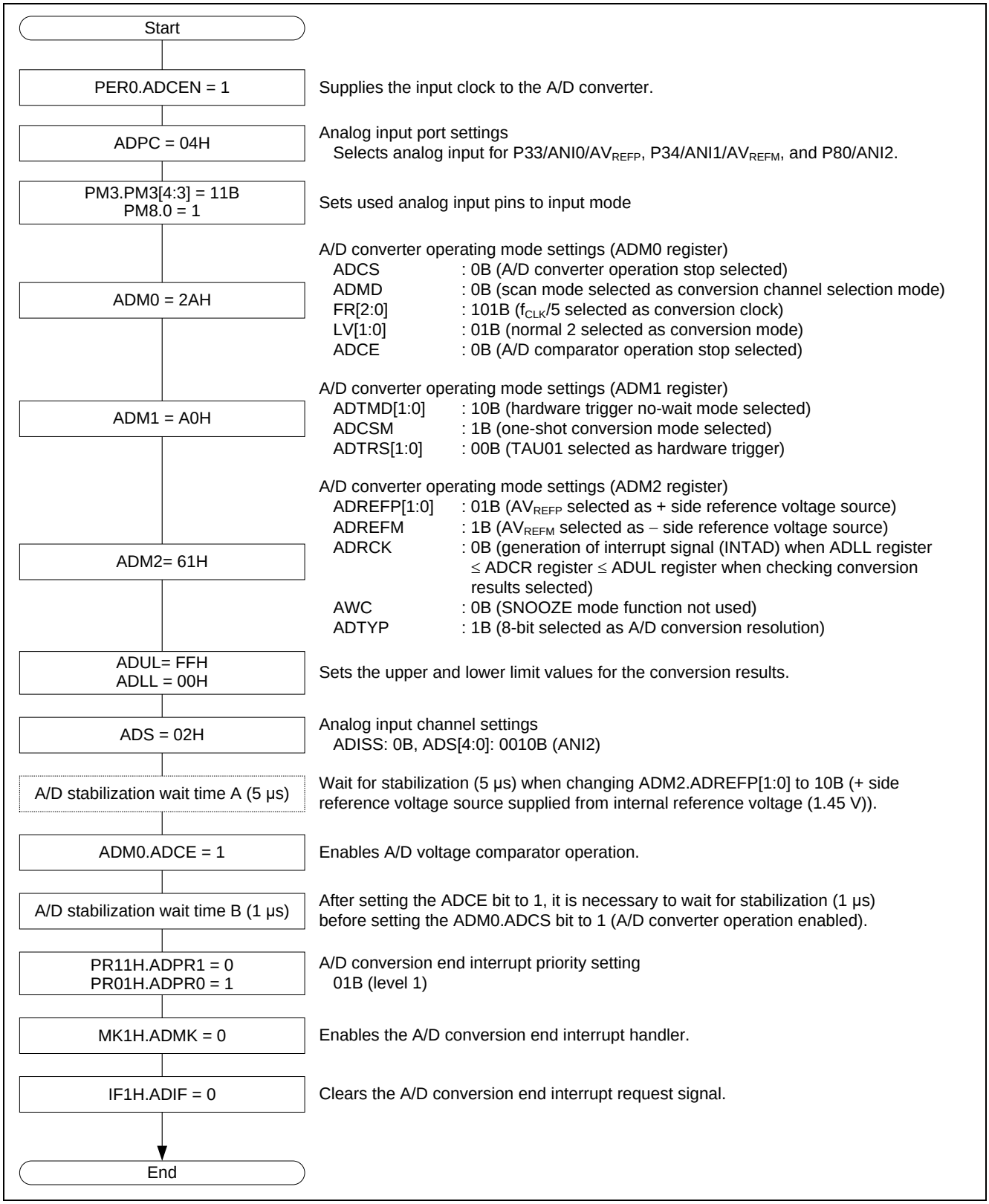
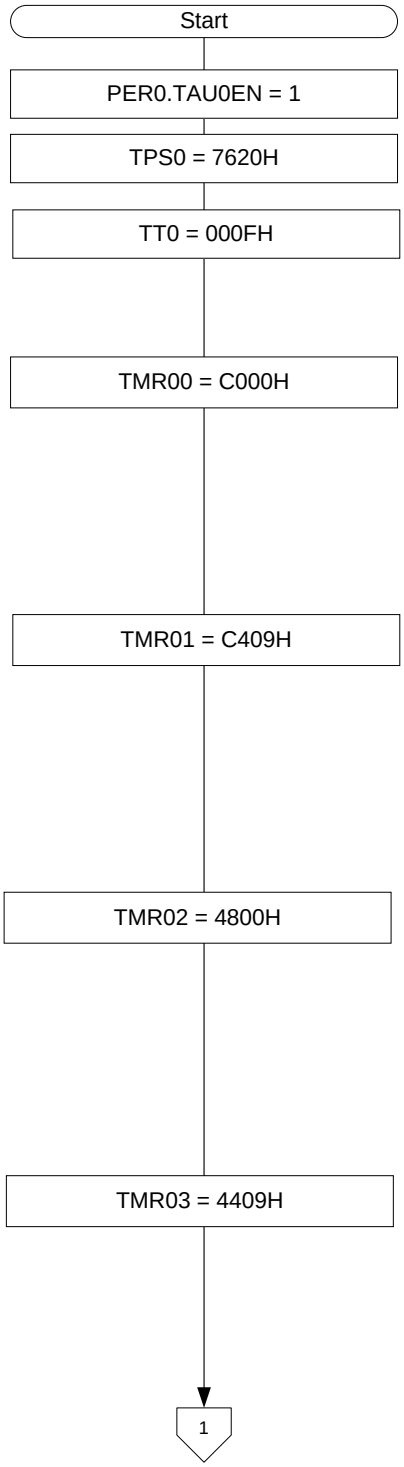


Figure 3.5 A/D Converter Initialization Procedure

3.4 TAU Initialization Procedure

TAU00 is set as a timer with a period of 2.04 ms and TAU01 is set to 1.02 ms as the slave channel of TAU00. Next, TAU02 is set as the master channel and TAU03 as the slave channel with a period of 510 µs for use as a PWM function.

Figure 3.6 and Figure 3.7 show the TAU initialization procedure.



Supplies the input clock to the TAU0.

TAU0 timer clock selections
CK00: f_{CLK}, CK01: f_{CLK}/4, CK02: f_{CLK}/64, CK03: f_{CLK}/128

Stops counting of timers TAU00, TAU01, TAU02, and TAU03

TAU00 timer operating mode settings
- CKS00[1:0] : 11B (CK03 selected as f_{MCK})
- CCS00 : 0B (f_{MCK} selected as count clock (f_{TCLK}))
- STS00[2:0] : 000B (software trigger selected as start trigger)
- CIS00[1:0] : 00B (falling edge selected as valid edge of TI00 pin signal)
- MD00[3:1] : 000B (interval timer mode selected)
- MD000 : 0B (interrupt not generated at count start)

TAU01 timer operating mode settings
- CKS01[1:0] : 11B (CK03 selected as f_{MCK})
- CCS01 : 0B (f_{MCK} selected as count clock (f_{TCLK}))
- SPLIT01 : 0B (16-bit timer, operates as slave channel)
- STS01[2:0] : 100B (master channel interrupt signal used as start trigger)
- CIS01[1:0] : 00B (falling edge selected as valid edge of TI00 pin signal)
- MD01[3:1] : 100B (one-count mode selected)
- MD010 : 1B (start trigger enabled and interrupts generated during count operation)

TAU02 timer operating mode settings
- CKS02[1:0] : 01B (CK02 selected as f_{MCK})
- CCS02 : 0B (f_{MCK} selected as count clock (f_{TCLK}))
- MASTER02 : 1B (operation as master for simultaneous channel operation function selected)
- STS02[2:0] : 000B (software trigger selected as start trigger)
- CIS02[1:0] : 00B (falling edge selected as valid edge of TI00 pin signal)
- MD02[3:1] : 000B (interval timer mode selected)
- MD020 : 0B (interrupt not generated at count start)

TAU03 timer operating mode settings
- CKS03[1:0] : 01B (CK02 selected as f_{MCK})
- CCS03 : 0B (f_{MCK} selected as count clock (f_{TCLK}))
- SPLIT03 : 0B (16-bit timer, operates as slave channel)
- STS03[2:0] : 100B (master channel interrupt signal used as start trigger)
- CIS03[1:0] : 00B (falling edge selected as valid edge of TI00 pin signal)
- MD03[3:1] : 100B (one-count mode selected)
- MD030 : 1B (start trigger enabled and interrupts generated during count operation)

To Figure 3.7, TAU Initialization Procedure (2/2)

Figure 3.6 TAU Initialization Procedure (1/2)

From figure 3.6, TAU Initialization Procedure (1/2)

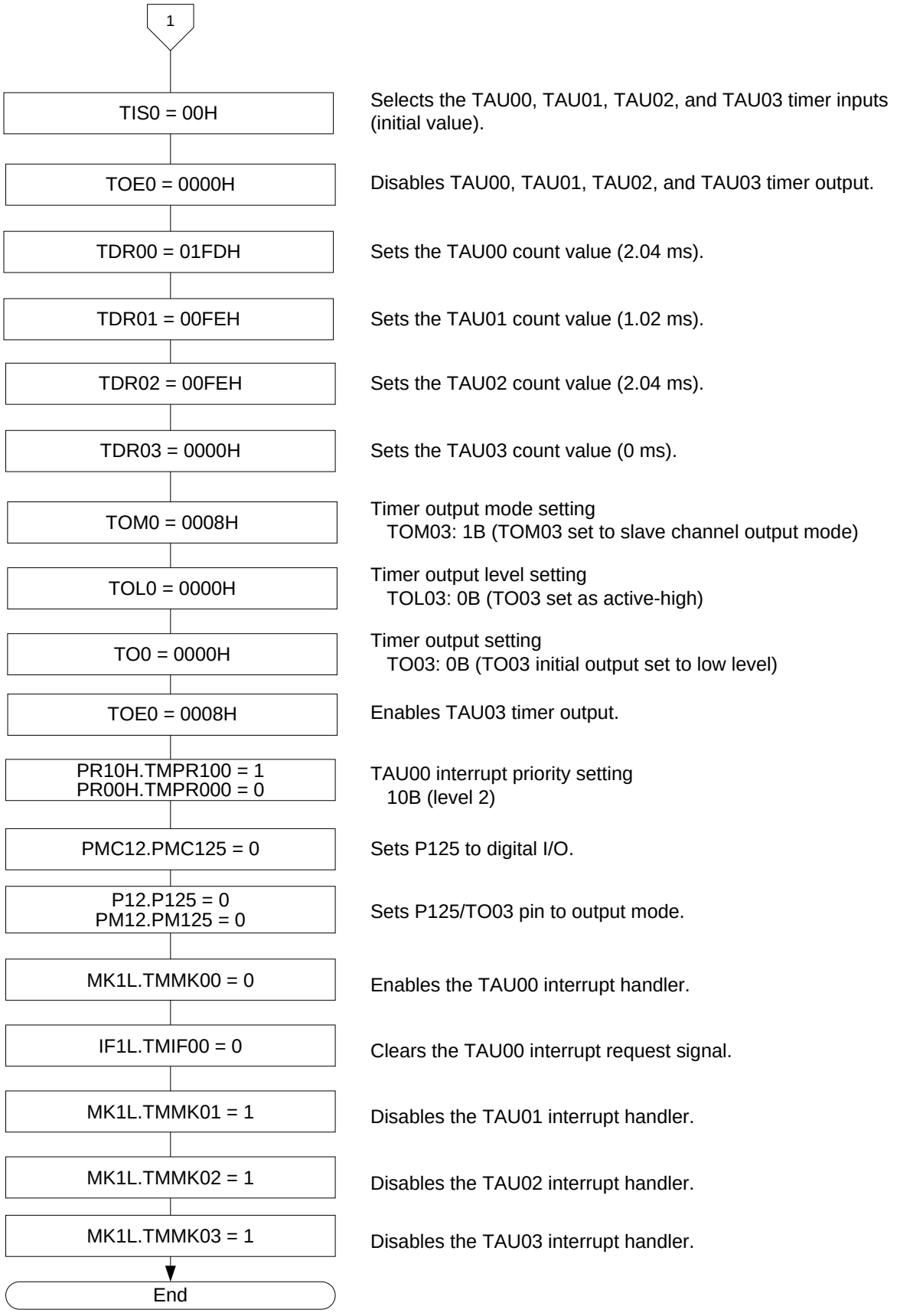


Figure 3.7 TAU Initialization Procedure (2/2)

3.5 SAU Initialization Procedure

Settings are made to enable SAU0 to transmit in UART mode.

Figure 3.8 shows the SAU initialization procedure.

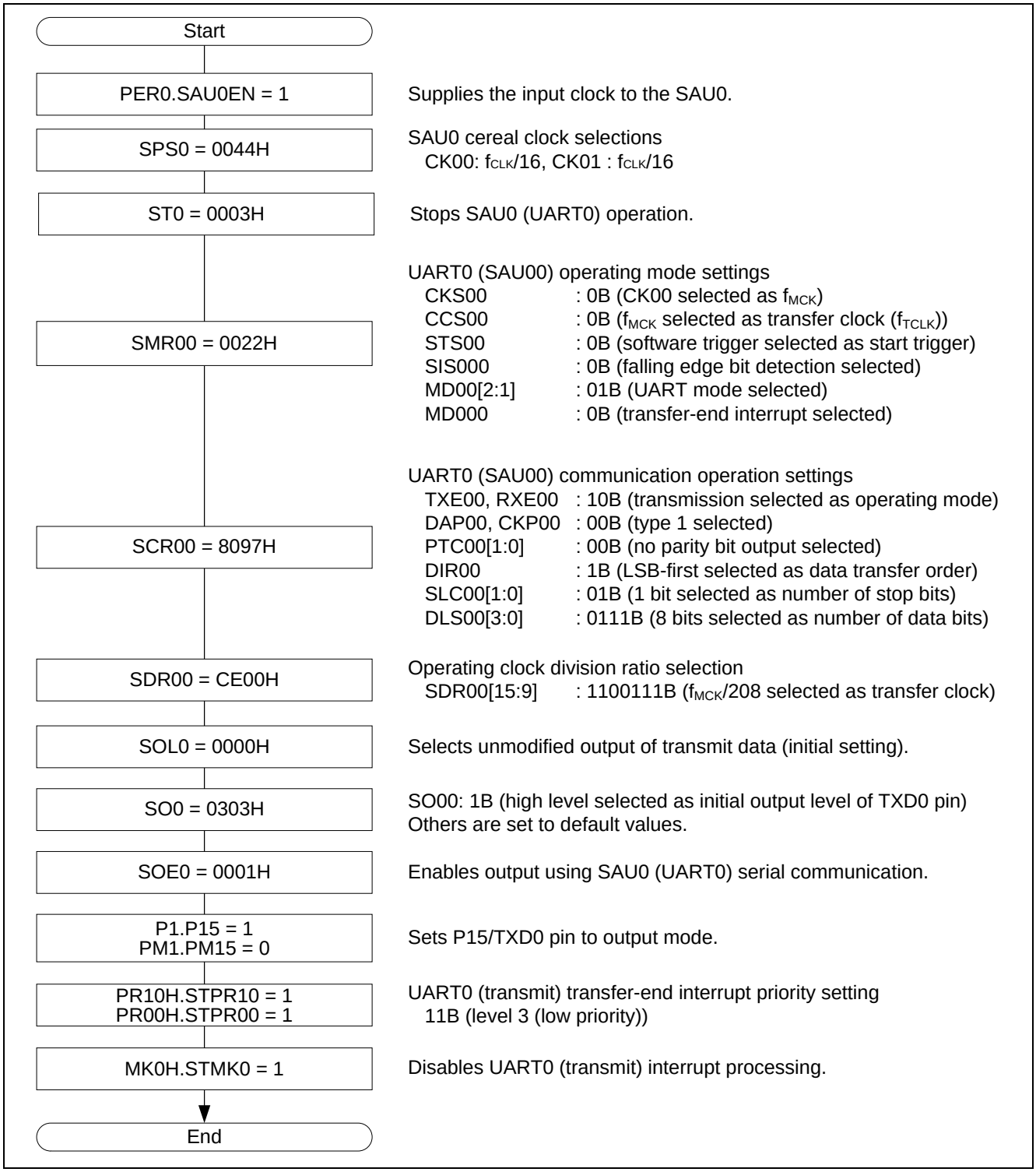
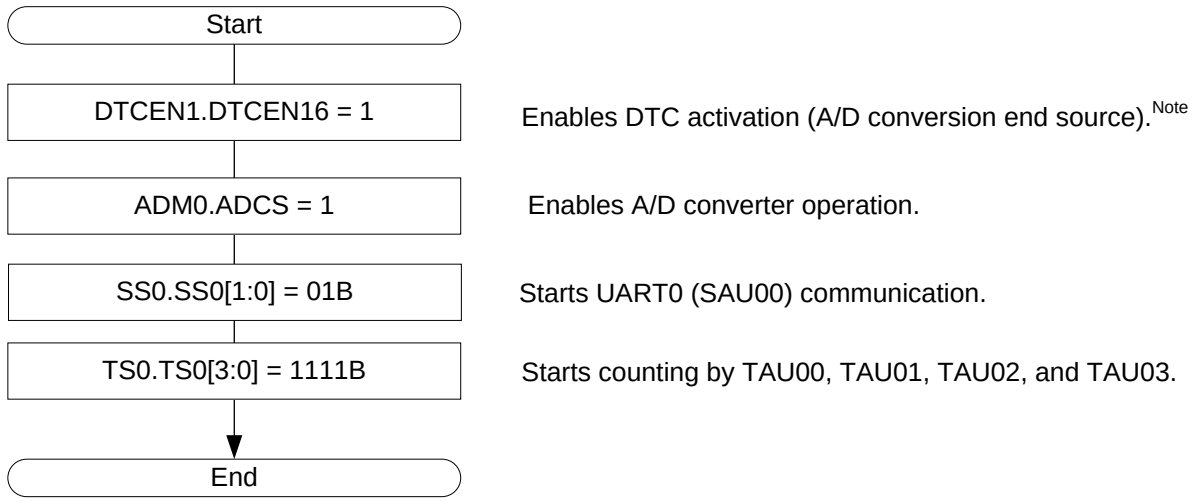


Figure 3.8 SAU Initialization Procedure

3.6 Procedure for Enabling Peripheral Functions (DTC (High-Speed Transfer) Transfer Start)

After initializing the peripheral functions (DTC, A/D converter, TAU, and SAU), the operation of the peripheral functions is enabled (started).

Figure 3.9 shows the procedure for enabling the operation of the peripheral functions (DTC (high-speed transfer) transfer start).

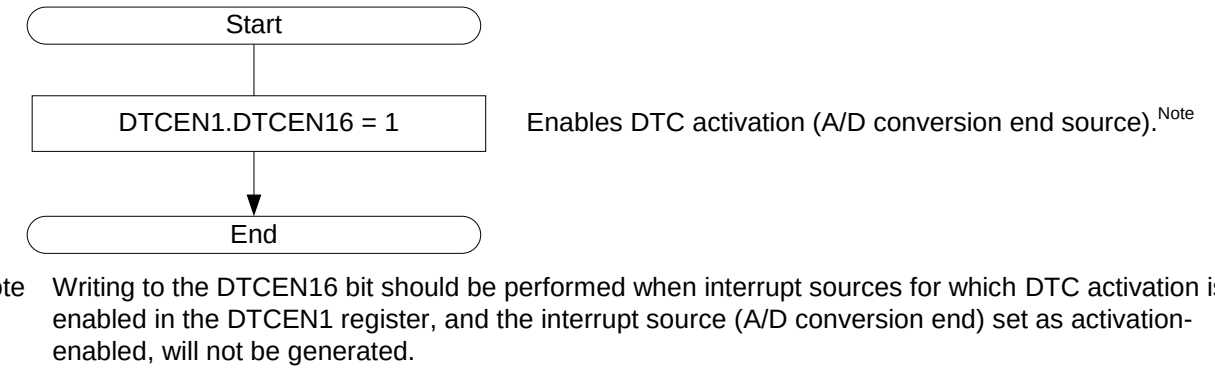


Note Writing to the DTCEN16 bit should be performed when interrupt sources for which DTC activation is enabled in the DTCEN1 register, and the interrupt source (A/D conversion end) set as activation-enabled, will not be generated.

Figure 3.9 Procedure for Enabling Peripheral Functions (DTC (High-Speed Transfer) Transfer Start)

3.7 DTC Transfer-End Interrupt Handler

When DTC transfer ends, the corresponding interrupt (in the example presented in this document, the A/D conversion-end interrupt) is generated. Figure 3.10 shows the handling of the DTC transfer-end interrupt (A/D conversion-end interrupt) in which the DTC transfer operation is re-enabled.



Note Writing to the DTCEN16 bit should be performed when interrupt sources for which DTC activation is enabled in the DTCEN1 register, and the interrupt source (A/D conversion end) set as activation-enabled, will not be generated.

Figure 3.10 DTC Transfer-End Interrupt (A/D Conversion End Interrupt) Handler

4. Important Points

4.1 DTC Transfer Cycle Count

The minimum number of transfer clock cycles is 8 for DTC (normal transfer) and 4 for DTC (high-speed transfer). Using the DTC specifications in the usage example presented in this document, each transfer (consisting of one high-speed transfer + two normal transfers executed as chain transfers) requires 20 clock cycles. For details, refer to Table 4.1.

Table 4.1 DTC Transfer Clock Cycle Count (Repeat Mode)

Transfer Type	Transfer Source	Transfer Destination	Vector Read	Control Data		Data Read	Data Write	Total
				Read	Write-Back			
High-speed transfer	ADCRH	RAM	1		1	1	1	4
Normal transfer	RAM	SDR00L	—	4	2	1	1	8
Normal transfer	RAM	TDR03	—	4	2	1	1	8

Note See Table 4.2 and Table 4.3 for the control data write-back clock cycle count, Table 4.4 and Table 4.5 for the data read clock cycle count, and Table 4.6 and Table 4.7 for the data write clock cycle count. The settings used in the example presented in this document are indicated in Table 4.2 to Table 4.7 by the white unshaded cells.

Table 4.2 Clock Cycle Count Necessary for DTC Control Data Write-Back

DTCCR register				Address Fixed/Incremented		Write-Back Control Data Area Registers				Clock Cycles
DAMOD	SAMOD	RPTSEL	MODE	Transfer Source	Transfer Destination	DTCCTj	DTRLDj	DTSARj	DTDARj	
0	0	X	0	Fixed	Fixed	Write-back	Write-back	—	—	1
0	1	X	0	Incremented	Fixed	Write-back	Write-back	Write-back	—	2
1	0	X	0	Fixed	Incremented	Write-back	Write-back	—	Write-back	2
1	1	X	0	Incremented	Incremented	Write-back	Write-back	Write-back	Write-back	3
0	X	1	1	Repeat	Fixed	Write-back	Write-back	Write-back	—	2
1	X	1	1	Repeat	Incremented	Write-back	Write-back	Write-back	Write-back	3
X	0	0	1	Fixed	Repeat	Write-back	Write-back	—	Write-back	2
X	1	0	1	Incremented	Repeat	Write-back	Write-back	Write-back	Write-back	3

Note X: 0 or 1, —: no write-back, j = 0 to 23

Table 4.3 Clock Cycle Count Necessary for DTC (High-Speed Transfer) Control Data Write-Back

HDTCCRm Register Settings				Address Settings		Write-Back Control Registers				Clock Cycles
HDAMODm	HSAMODm	HRPTSELm	HMODEm	Transfer Source	Transfer Destination	HDTCCTm	HDTRLDm	HDTSARm	HDTDARm	
0	0	X	0	Fixed	Fixed	Write-back	—	—	—	1
0	1	X	0	Incremented	Fixed	Write-back	—	Write-back	—	1
1	0	X	0	Fixed	Incremented	Write-back	—	—	Write-back	1
1	1	X	0	Incremented	Incremented	Write-back	—	Write-back	Write-back	1
0	X	1	1	Repeat	Fixed	Write-back	—	Write-back	—	1
1	X	1	1	Repeat	Fixed	Write-back	—	Write-back	Write-back	1
X	0	0	1	Fixed	Repeat	Write-back	—	—	Write-back	1
X	1	0	1	Incremented	Repeat	Write-back	—	Write-back	Write-back	1

Note X: 0 or 1, —: no write-back, m = 0 or 1

Table 4.4 DTC Data Read Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
1	2	4	1	1	1 + wait cycle count

Note A wait of one clock cycle is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

Table 4.5 DTC (High-Speed Transfer) Data Read Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
—	—	—	1	1	1 + wait cycle count

Note A wait of one clock cycle is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

Table 4.6 DTC Data Write Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
1	—	—	1	1	1 + wait cycle count

Note A wait of one clock cycle is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

Table 4.7 DTC (High-Speed Transfer) Data Write Clock Cycle Count

RAM	Flash Memory		SFR		
	Code Flash	Data Flash	1st SFR	2nd SFR (No Wait)	2nd SFR (Wait)Note
1	—	—	1	1	1 + wait cycle count

Note A wait of one clock cycle is necessary when accessing the CAN- and LIN-related registers and the TRJ0 register of timer RJ.

4.2 DTC Usage Notes

- Do not use a DTC transfer to access DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCCTm, HDTRLDm, HDTSARm, and HDTDARm) or the DTC control data area, DTC vector table area, or general-register (FFEE0H-FFEFFH) space in the RAM. Also, when using self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function, do not access the memory areas associated with those functions.
- Write to or change the DTCENi register only when the interrupt sources for which the DTC activation is enabled in the target register, and the interrupt sources set as activation-enabled will not be generated.
- Do not use the memory areas associated with the general-register (FFEE0H-FFEFFH) space, self-programming, the data flash libraries, the on-chip trace function, or the hot plugin function as the DTC control data area or DTC vector table area.
- Only make changes to the DTC-related registers (DTCBAR, SELHSm, HDTCCRm, HDTCCTm, HDTRLDm, HDTSARm, and HDTDARm), the registers assigned to the DTC control data area (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj), and the DTC vector table area when all DTC activation sources are set as activation-disabled (corresponding bits in DTCENi register cleared to 0).
- Make initial settings (write random values) to the DTC control data area and DTC vector table area in the RAM. The DTC vector table area (64 bytes; including reserved areas) must not be used as general-purpose RAM by user programs. Note that portions of the DTC control data area (192 bytes) that are not used by the DTC can be used as general-purpose RAM.
- Do not overwrite DTCBAR more than once.
- When a DTC transfer-pending instruction (call or return instruction, unconditional or conditional branch instruction, instruction for accessing code flash memory, instruction for accessing interrupt-related registers (IFxx, MKxx, and PRxx) or PSW, instruction for accessing the data flash, or multiply, divide, or multiply-and-accumulate instruction - except for the MULU instruction) is executed, the DTC transfer does not take place and the request is put on hold. Also, no DTC transfer takes place during a PREFIX instruction and for a period equal to one instruction immediately following it.
- If a data flash access instruction is executed during the period equal to one instruction after the activation of a DTC data transfer, a wait of three clock cycles occurs due to the specifications of the internal bus.
- The DTC transfer is put on hold when an access is made to an SFR requiring a wait (CAN or LIN register, or the TRJ0 register of timer RJ).
- From the point at which a DTC activation source is generated until the point at which the DTC transfer completes, the same activation source should not be generated again.
- If there is a conflict between DTC activation sources, the priorities of the activation sources are considered. The source with the higher priority (based on the source number) takes effect, and the source with the lower priority is put on hold.
- In order to read from the DTC control data area and DTC vector table area during high-speed transfer operation, write random values to them before enabling DTC transfer operation.
- In repeat mode, the lower byte of the address (setting value) of the repeat area must have a value of 00H. Also note that the transfer count and reload transfer count will differ according to the transfer data size.
  - 8-bit transfer: 01H to FFH (1 to 255 times)
  - 16-bit transfer: 01H to 7FH (1 to 127 times)

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Revision History

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		Page	Summary
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